

## ARINC 818 Transceiver Core

## Product Brief

Available Q2 2008

### Description

Great River Technology's (GRT) ARINC 818 transceiver core provides an easy way to implement ARINC 818 compliant interfaces in Xilinx V2Pro and V5 PLDs. The core uses Xilinx Rocket IO transceivers (MGTs or GTP tiles) to achieve ARINC 818 interfaces up to 3.1875 Gbps (4.25 Gbps coming soon). The core can be used for transmit only, receive only, or for transmit and receive applications.

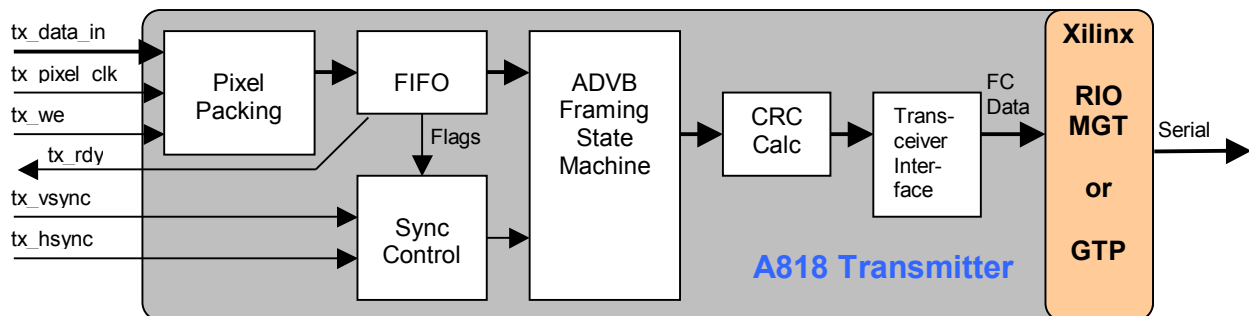
The core has many flexible compile time settings allowing for various link speeds, line segmentations, and line synchronization methods. The core can be configured for various resolutions and pixel packing methods. Ancillary data can use default values set at compile time or data can be updated in real time via register interface.

### Features

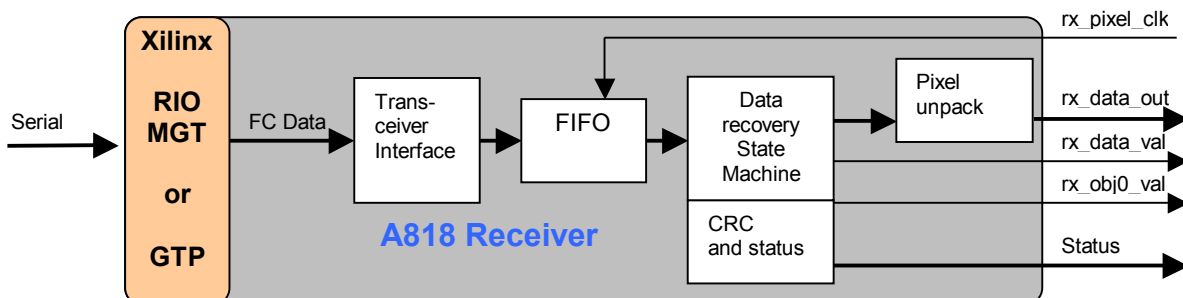
- Supports link speeds up to 3.1875 Gbps
- Flexible video resolution/frame rates
- Compatible with progressive and interlaced video
- Simple pixel bus transmitter interface
- Configurable for various pixel packing and input formats
- Supports line synchronous transmission
- Embedded ancillary data with real time update
- Compatible with in Xilinx V2Pro and V5 PLDs
- Configurable for various line segmentations
- Receiver error and status detection
- Complete Header/Ancillary data recovery
- Low Latency

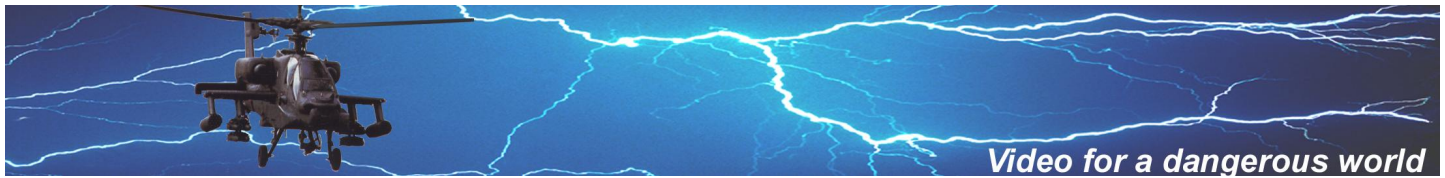
### Block Diagram

The transmitter has a simple interface where native Vsync, Hsync, and pixel clocks can be used. Out-going ARINC 818 frames are governed by this input timing. Internal FIFOs allow writing of continuous line data without hold off, therefore, the core can be tied directly to pixel buses with various timings (such as VESA timings). The core supports various color input formats (up to 32-bit RGBA) and monochrome formats (up to 16-bits). Internal pixel packing logic can be configured to compress data prior to transmission.

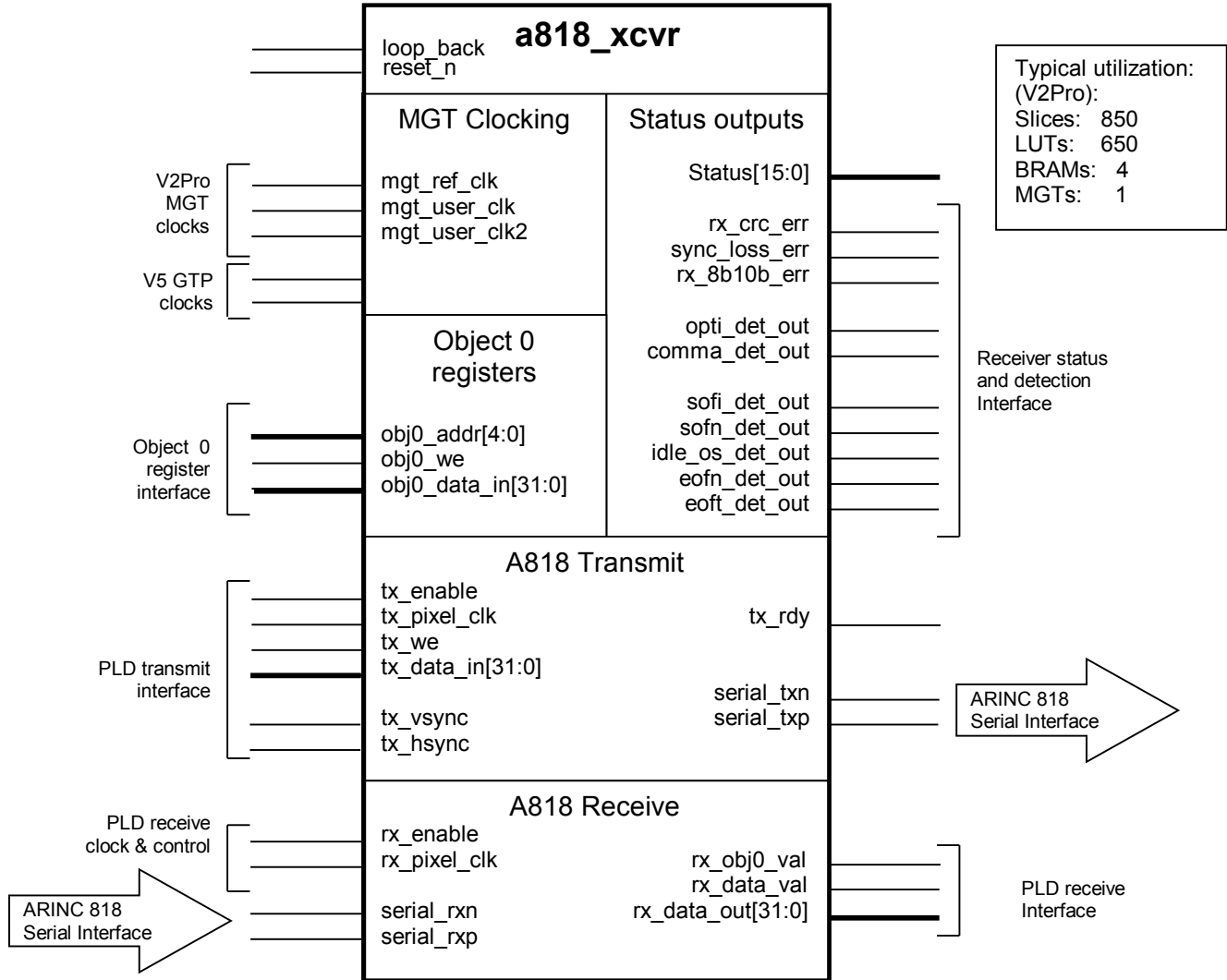


The receiver is configurable for unpacking pixel data in several formats. The PLD interface is a 32-bit wide data bus with a simple data valid signal. The core has internal receiver FIFOs so that the Pixel clock rate can be set by the user.





## ARINC 818 Tranceiver Core Pin Diagram



## Deliverables & Options

- VHDL and Encrypted VHDL files
- Instantiation templates
- VHDL test bench
- UCF file templates
- Coregen output files
- User's Guide
- Optional Aerospace Certification Package
- Optional Chipset and Reference Design

## How to Buy:

GRT licenses the ARINC 818 core on a project basis using a Sign Once™ agreement. Additionally, VHDL source code and a complete Aerospace Certification Package may also be purchased to support DO 254 qualification. GRT also offers development boards, design support and engineering services for customization of the core. For more information contact Great River Technology at: (505) 881-6262 or [sales@GreatRiverTech.com](mailto:sales@GreatRiverTech.com)